Refine Search

Search Results -

Terms	Documents
L2 same hot	37

Database:

- US Pre-Grant Publication Full-Text Database
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- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, July 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	L2 same hot	37	L4
L3	L2 same "hot-plug"	2	L3
L2	sens$3 near5 (insert$3 or remov$3) near10 signal	5598	L2
L1	sens$3 same (insert$3 or remov$3) same signal	69809	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L4	0

Database:
US Pre-Grant Publication Full-Text Database
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IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, July 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L4	0	L5
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	L2 same hot	37	L4
L3	L2 same "hot-plug"	2	L3
L2	sens$3 near5 (insert$3 or remov$3) near10 signal	5598	L2
L1	sens$3 same (insert$3 or remov$3) same signal	69809	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
4941841.pn. or 5010426.pn. or 5045960.pn. or 5717571.pn. or 5721669.pn. or 6266724.pn. or 6131134.pn.	7

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
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EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, July 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L1	4941841.pn. or 5010426.pn. or 5045960.pn. or 5717571.pn. or 5721669.pn. or 6266724.pn. or 6131134.pn.	7	L1

END OF SEARCH HISTORY

Freeform Search

Database: US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
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EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term: L1 and (signal same (insert$3 or remov$3))

Display: 10 **Documents in Display Format:** TI **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

DATE: Friday, July 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L4	L1 and (signal same (insert$3 or remov$3))	1	L4
L3	L1 and (sens$3 same (insert$3 or remov$3))	1	L3
L2	L1 and (sens$3 near5 (insert$3 or remov$3))	0	L2
L1	4941841.pn. or 5010426.pn. or 5045960.pn. or 5717571.pn. or 5721669.pn. or 6266724.pn. or 6131134.pn.	7	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(710/301 |710/302).ccls. and ((sens$3 near5 (insert$3 or remov$3)) same signal)	26

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, July 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L6	710/301-302.ccls. and ((sens$3 near5 (insert$3 or remov$3)) same signal)	26	L6
L5	710/301-302.ccls. and (sens$3 near5 (insert$3 or remov$3))	48	L5
L4	L1 and (signal same (insert$3 or remov$3))	1	L4
L3	L1 and (sens$3 same (insert$3 or remov$3))	1	L3
L2	L1 and (sens$3 near5 (insert$3 or remov$3))	0	L2
L1	4941841.pn. or 5010426.pn. or 5045960.pn. or 5717571.pn. or 5721669.pn. or 6266724.pn. or 6131134.pn.	7	L1

END OF SEARCH HISTORY

Results for "(sens* and insert* and hot and signal and control*<in>metadata) <and> (remov*<in&..."

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Your search matched **10** of **1189536** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» View Session History

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Modify Search

(sens* and insert* and hot and signal and control*<in>metadata) <and> (remov*<in> >>

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **Rule-based autotuning based on frequency domain identification**
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9. **The MD 122 dual 3 Mbyte flexible disk drive**
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23-25 Sept. 1997 Page(s):2 - 7
AbstractPlus | Full Text: PDF(700 KB) IEEE CNF

The MD 122 dual 3 Mbyte flexible disk drive

Stewart, A.
Burroughs Machines Ltd., Glenrothes, Scotland

This paper appears in: **Magnetics, IEEE Transactions on**
Publication Date: Jul 1981
Volume: 17 , Issue: 4
On page(s): 1403 - 1407
ISSN: 0018-9464
Posted online: 2003-01-06 16:52:34.0

Abstract
The dual 3Mbyte flexible disk drive provides 6 Mbyte of formatted data storage in a compact package designed for in-built use. The two disks may be **inserted** or **removed** independently and share a common double ended spindle. A common actuator is used to position the four recording heads. High areal recording density is achieved using advanced technology recording heads and media in association with a microprocesor **controlled** environmentally compensated servo positioner. The drive incorporates an intelligent **controller** which provides sophisticated data handling functions and **controls** the drive in such a manner that the interface to the host is free of drive dependant parameters.

Index Terms
Inspec
Controlled Indexing
Not Available

Non-controlled Indexing
Magnetic disk recording
Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

L4: Entry 17 of 37 File: USPT Jul 10, 2001

DOCUMENT-IDENTIFIER: US 6260155 B1
TITLE: Network information server

Brief Summary Text (14):
The invention accordingly provides for an information server system having a scalable, modular, fault tolerant, hot swappable architecture of a plurality of components for interfacing with a computer network such as the Internet, comprising a central processing unit, a communications interface subsystem connected to the central processing unit, a mass storage subsystem connected to the central processing unit, and a diagnostics computer subsystem connected to the central processing unit for monitoring when one of the plurality of components of the information server system is removed or added. In a presently preferred embodiment, the information server system further comprises a mid-plane connector board having a plurality of sockets for connecting the components on each side of the mid-plane connector board, and the components of the information server system are currently preferably connected to the mid-plane connector board of the information server system by interface cards. In a preferred aspect of the invention, the interface cards comprise circuitry to sense when the interface cards are failing or are being removed, and to generate a signal to the diagnostics subsystem of the information server system indicating that the component connected to the connector board by the interface card is to be taken off line, to allow the information server system to switch the components off as they are taken off-line, and to switch them on as they are placed on-line, allowing the information system to be fully hot-swappable. Each the component preferably has a unique electronic serial number recognized by the diagnostics subsystem, allowing the components to be integrated into the information server system.

Brief Summary Text (16):
In one presently preferred embodiment, the mass storage subsystem comprises a plurality of disk storage devices, and each of the plurality of disk storage devices is mounted on a bypass interface card that connects to a mid-plane connector board having a plurality of sockets for connecting interface cards for components on each side of the mid-plane connector board. The bypass interface cards are sequentially connectable together by jumper cables, so that a plurality of disk storage devices can be connected together. In a currently preferred aspect, the bypass interface cards include circuitry to sense when a bypass interface card is failing or is being removed, and to generate a signal to the diagnostics subsystem of the information server system indicating that the disk storage device connected to the connector board by the bypass interface card is to be taken off line, to allow the information server system to switch the disk storage components off as they are taken off-line, and to switch them on as they are placed on-line, allowing the information system to be fully hot-swappable. In one presently preferred embodiment, the mass storage subsystem comprises a fibre channel disk storage device array subsystem.

Detailed Description Text (6):
Each mid-plane connector board advantageously has sockets 28 for connecting interface cards for components on each side of the mid-plane connector board, and each mid-plane connector board further can have upper and lower sets of sockets, allowing for components to be mirrored left and right, and top and bottom, to significantly increase fault tolerance of the information server system. Multiple mid-plane connector boards can be utilized in the information server system, allowing for expansion and scalability of the system. Each of the bypass interface cards are sequentially connectable together by jumper cables, so that any number of disk storage. devices can be connected together to make the configuration scalable to up to any needed mass storage configuration, limited only by the size of space available for disk storage provided by the physical server case framework. As is further explained in greater detail below, the diagnostics subsystem monitors the serial numbers for the components on-line, and monitors when a component is removed or added. Each bypass interface card preferably includes

circuitry to sense when a bypass interface card is failing or is being removed, and to generate a signal to the diagnostics subsystem of the information server system indicating that the individual is to be taken off line, to allow the information server system to switch the disk storage components off as they are taken off-line, and to switch them on as they are placed on-line, allowing the information system to be fully hot-swappable.

CLAIMS:

3. The information server system of claim 2, wherein said interface cards comprise circuitry to sense when the interface cards are failing or is being removed, and to generate a signal to the diagnostics subsystem of the information server system indicating that the component connected to the connector board by the interface card is to be taken off line, to allow the information server system to switch the components off as they are taken off-line, and to switch them on as they are placed on-line, allowing the information system to be fully hot-swappable.

11. The information server system of claim 10, wherein each of said bypass interface cards include circuitry to sense when a bypass interface card is failing or is being removed, and to generate a signal to the diagnostics subsystem of the information server system indicating that the disk storage device connected to the connector board by the bypass interface card is to be taken off line, to allow the information server system to switch the disk storage components off as they are taken off-line, and to switch them on as they are placed on-line, allowing the information system to be fully hot-swappable.

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L4: Entry 17 of 37 File: USPT Jul 10, 2001

US-PAT-NO: 6260155
DOCUMENT-IDENTIFIER: US 6260155 B1

TITLE: Network information server

DATE-ISSUED: July 10, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dellacona; Richard	Riverside	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
QUAD Research	Riverside	CA			02

APPL-NO: 09/ 071282 [PALM]
DATE FILED: May 1, 1998

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/4; 714/46
US-CL-CURRENT: 714/4; 714/46

FIELD-OF-SEARCH: 714/2, 714/4, 714/6, 714/7, 714/8, 714/13, 714/14, 714/25, 714/30, 714/39, 714/46, 714/47, 370/220, 370/226, 709/238, 709/239, 709/242, 710/102, 710/103, 380/255, 702/130, 702/142, 702/146, 375/354

PRIOR-ART-DISCLOSED:

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Search Selected Search ALL Clear

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0 760 503 A1	March 1997	EP	

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ART-UNIT: 211

PRIMARY-EXAMINER: Trammell; James P.

ASSISTANT-EXAMINER: Elisca; Pierre Eddy

ATTY-AGENT-FIRM: Fulwider, Patton Lee & Utecht

ABSTRACT:

The information server system provides a scalable expansion capability, due to the implementation of a unique mid-plane connector board for all components of the information server system that allows for multiply mirrored components to significantly improve fault tolerance of the server system. An integrated diagnostics monitoring subsystem eliminates the incompatability problems previously associated with performing diagnostics of the server system. A method is also provided for increasing the throughput rate of the user communications interface by installing a hash table database in the end user computer system to bypass a similar but slower function in the end user modem, to place the bulk of the transmission reception load on the main CPU, and synchronizing the modem with the transmission speed of the server unit.

18 Claims, 7 Drawing figures

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L4: Entry 9 of 37 File: PGPB Dec 19, 2002

DOCUMENT-IDENTIFIER: US 20020194548 A1
TITLE: Methods and apparatus for computer bus error termination

Summary of Invention Paragraph:
[0007] In one embodiment, the isolation control logic receives the device isolation signal from system software. In another embodiment, for a system using virtual memory addressing, the isolation control logic receives the device isolation signal from input/output virtual address (IOVA) error detector detecting bus transactions addressing an invalid memory location. In another embodiment, the isolation control logic receives the device isolation signal from protocol checker logic monitoring the validity of the protocol for each of the bus transactions. In yet another embodiment, the isolation control logic receives the device isolation signal from a hot-plug sensor element responsive to the physical removal of the device from its bus interface slot.

Detail Description Paragraph:
[0035] In one embodiment, a hot-plug sensor 48 is provided to sense the physical removal of the device 32 from its bus interface slot. When the device 32 is extracted from its bus interface slot the device 32 must be isolated from the bus as described herein to avoid causing a bus fault. The sensor hot-plug 48 senses that the device 32 is being physically removed from its bus interface slot. In response to sensing the physical removal of the device 32, the hot-plug sensor 48 transmits the ISOLATE signal to the isolation control logic 36. The isolation control logic 36 response to the ISOLATE signal by commanding the isolation of the device 32 from the bus 12 as previously described.

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First Hit Previous Doc Next Doc Go to Doc#

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L4: Entry 9 of 37 File: PGPB Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020194548
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020194548 A1

TITLE: Methods and apparatus for computer bus error termination

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Tetreault, Mark	Webster	MA	US	

APPL-NO: 09/ 871180 [PALM]
DATE FILED: May 31, 2001

INT-CL: [07] H04 L 1/22

US-CL-PUBLISHED: 714/43
US-CL-CURRENT: 714/43

REPRESENTATIVE-FIGURES: 2

ABSTRACT:

In a computer system having a bus architecture, a system and process for isolating a device from a bus without interrupting system operation is described, the system including bus interface logic monitoring and reporting activity on the bus, isolation control logic receiving error signals from error detectors, and isolation switches through which devices are interconnected to the bus, the isolation switches allowing for the isolation of the devices from the bus. The isolation control logic determines the devices to be isolated responsive to the reported error and, in turn, transmits an isolation switch control signal to the isolation switch(es) associated with the identified device(s) to isolate those device(s) from the bus. In some embodiments, errors are reported by system software, input/output virtual address error detectors for systems using virtual memory addressing, protocol error detectors, and sensors sensing the physical removal of a bus-connected device from its bus interface slot.

Previous Doc Next Doc Go to Doc#

L4: Entry 7 of 37 File: PGPB Sep 9, 2004

DOCUMENT-IDENTIFIER: US 20040177202 A1
TITLE: Apparatus and method for generating hot-plug signal

Abstract Paragraph:
An apparatus and method for recognizing whether a medium is inserted into or removed from a hot-plug apparatus and generating a hot-plug signal are provided. The hot-plug signal generation apparatus includes a medium insertion unit, which receives a medium and generates a sensor signal when the medium is inserted or removed; a medium control unit which controls the received medium and generates the hot-plug signal; and a switch which outputs the hot-plug signal in response to the sensor signal generated by the medium insertion unit.

Summary of Invention Paragraph:
[0017] According to an exemplary aspect of the present invention, there is provided an apparatus for generating a hot-plug signal comprising: a medium insertion/removal sensing unit which senses when a medium is inserted or removed; and a hot-plug signal control unit which outputs a hot-plug signal when the medium insertion/removal sensing unit senses that the medium is inserted or removed.

Summary of Invention Paragraph:
[0018] According to another exemplary aspect of the present invention, an apparatus for generating a hot-plug signal comprises: a medium insertion unit, which receives a medium and generates a sensor signal when the medium is inserted or removed; a medium control unit which controls the received medium and generates a hot-plug signal; and a switch which outputs the hot-plug signal in response to the sensor signal generated by the medium insertion unit.

Summary of Invention Paragraph:
[0020] According to still another exemplary aspect of the present invention, there is provided a method for generating a hot-plug signal comprising: (a) sensing when a medium is inserted or removed; and (b) controlling a hot-plug signal to be output or not so that the hot-plug signal is output when the medium is inserted or removed.

Summary of Invention Paragraph:
[0021] According to yet another exemplary aspect of the present invention, a method for generating a hot-plug signal comprises: (a) generating a sensor signal when a medium is inserted or removed; (b) controlling the medium and generating a hot-plug signal, and (c) controlling a hot-plug signal to be output in response to the sensor signal.

Detail Description Paragraph:
[0030] The memory stick insertion unit 210, which is also referred to as a medium insertion/removal sensing unit, is a portion into which a memory stick 250 is inserted and has signal lines that are determined according to an interface with the memory stick 250. For example, a pin number five of the memory stick 250 and a corresponding pin of the interface of the memory stick insertion unit 210 become low upon insertion of the memory stick 250. This connects the pin number five of the memory stick 250 to the switch 230 to switch a D+ or D- signal of USB, thus generating a hot-plug signal. This uses a property of the memory stick 250 and the fact that a signal recognizing devices in USB is the D+ or D- signal.

Detail Description Paragraph:
[0033] In a case of a general external medium other than the memory stick, an apparatus for generating a hot-plug signal may include a medium insertion/removal sensing unit and a hot-plug signal control unit, wherein the medium insertion/removal sensing unit generates a signal when it senses that the external medium is inserted or removed, and the hot-plug signal control unit controls a hot-plug signal output according to the signal generated by the medium

insertion/removal sensing unit.

Detail Description Paragraph:
[0036] Then, the external medium is controlled and a hot-plug signal is generated (S320). The hot-plug signal may be a D+ or D- signal defined in a USB standard. Finally, an on/off operation of the hot-plug signal output is controlled in response to the sensor signal generated upon insertion/removal of the external medium (S330).

CLAIMS:

1. An apparatus for generating a hot-plug signal comprising: a medium insertion/removal sensing unit which senses when a medium is inserted or removed; and a hot-plug signal control unit which outputs a hot-plug signal when the medium insertion/removal sensing unit senses that the medium is inserted or removed.

2. An apparatus for generating a hot-plug signal comprising: a medium insertion unit, which receives a medium and generates a sensor signal when the medium is inserted or removed; a medium control unit which controls the received medium and generates a hot-plug signal; and a switch which outputs the hot-plug signal in response to the sensor signal generated by the medium insertion unit.

8. A method for generating a hot-plug signal comprising: (a) sensing when a medium is inserted or removed; and (b) controlling a hot-plug signal output so that the hot-plug signal is output when the medium is inserted or removed.

9. A method for generating a hot-plug signal comprising: (a) generating a sensor signal when a medium is inserted or removed; (b) controlling the medium and generating a hot-plug signal; and (c) controlling the hot-plug signal to be output in response to the sensor signal.

12. The method of claim 9, wherein in step (a), the sensor signal generated upon the insertion/removal of the medium is transferred to a switch for outputting the hot-plug signal.

15. A computer readable medium storing a computer program for executing a hot-plug signal generation method, the hot-plug signal generation method comprising: (a) sensing when a medium is inserted or removed; and (b) controlling a hot-plug signal output so that the hot-plug signal is output when the medium is inserted or removed.

16. A computer readable medium storing a computer program for executing a hot-plug signal generation method, the hot-plug signal generation method comprising: (a) generating a sensor signal by sensing whether a medium is inserted or removed; (b) controlling the medium and generating the hot-plug signal; and (c) controlling the hot-plug signal to be output in response to the sensor signal.

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Refine Search

Search Results -

Terms	Documents
L2 and (710/301 |710/302 |710/303 |710/304).ccls.	13

Database:

- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L8

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, July 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L8	L2 and 710/301-304.ccls.	13	L8
L7	L2 and 710/302-304.ccls.	7	L7
L6	L2 same 710/302-304.ccls.	0	L6
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L4	0	L5
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	L2 same hot	37	L4
L3	L2 same "hot-plug"	2	L3
L2	sens$3 near5 (insert$3 or remov$3) near10 signal	5598	L2
L1	sens$3 same (insert$3 or remov$3) same signal	69809	L1

END OF SEARCH HISTORY

L8: Entry 13 of 13 File: USPT Jun 3, 1997

DOCUMENT-IDENTIFIER: US 5636347 A
TITLE: Computer card insertion detection circuit

Current US Original Classification (1):
710/302

CLAIMS:

1. A card insertion detection apparatus for providing a warning signal to a host system that a circuit card is in the process of being inserted into a card slot of the host system in order to allow the host system to accept the circuit card in an orderly manner that does not adversely affect the host system by protecting the host system from transients that could result from the connection of the circuit card, the circuit card having a connector with a multiplicity of terminals distributed along the connector's width, and arranged in at least one row, for connecting to corresponding terminals of a mating connector in a host system card slot, the circuit card connector having a group of preassigned ground terminals located near both edges of the connector width, a subset of the group of ground terminals located near both edges being card insertion detection terminals to be used for card insertion detection, the apparatus comprising:

(a) a card slot connector with connector terminals for mating the card slot connector terminals with a circuit card connector terminals;

(b) detection circuitry connected to a subset of the card slot connector terminals corresponding to the card insertion detection terminals of the card slot connector for generating the warning signal indicating the onset of a circuit card insertion by sensing the grounding of at least one terminal of the card slot connector terminals; and

(c) grounding circuitry that grounds at least one card insertion detection terminal after the circuit card insertion is detected.

9. A system for detecting an insertion of a circuit card into a host system and for providing the host system with a warning signal that the circuit card is in the process of being inserted into the host system to allow the host system to accept the circuit card in an orderly manner that does not adversely affect the host system by protecting the host system from transients that could result from connection of the circuit card,

the circuit card comprising:

a connector having a multiplicity of terminals distributed along the width of a circuit card connector, and arranged in at least one row, for connecting to the corresponding terminals of a mating connector in a host system card slot; and

a group of preassigned ground terminals located near both edges of the connector width, a subset of the group of ground terminals located near both edges being card insertion detection terminals to be used for card insertion detection;

the host system comprising:

a card slot for the insertion of the circuit card, the card slot having the mating connector containing terminals to mate with the circuit card;

detection circuitry connected to a subset of the card slot connector terminals corresponding to the card insertion detection terminals of the card slot connector for generating the warning signal indicating the onset of a circuit card insertion by sensing the grounding of at least one terminal of the card slot connector terminals; and

grounding circuitry that grounds at least one card insertion detection terminal after the circuit card insertion is detected.

10. A means for providing a warning signal to a host system upon detection of a circuit card being inserted into a card slot of the host system in order to allow the host system to accept the circuit card in an orderly manner that does not adversely affect the host system by protecting the host system from transients that could result from the connection of the circuit card, the circuit card having a connector with a multiplicity of terminals distributed along the connector's width, and arranged in at least one row, for connecting to corresponding terminals of a mating connector in a host system card slot, the circuit card connector having a group of preassigned ground terminals located near both edges of the connector width, a subset of the group of ground terminals located near both edges being card insertion detection terminals to be used for card insertion detection, the means for detection comprising:

(a) a means for mating the host system card slot connector terminals with the circuit card connector terminals;

(b) detection means connected to a subset of the card slot connector terminals corresponding to the card insertion detection terminals of the card slot connector for generating the warning signal indicating the onset of a circuit card insertion by sensing the grounding of at least one terminal of the card slot connector terminals; and

(c) grounding means that grounds at least one card insertion detection terminal after the circuit card insertion is detected.

13. A card insertion detection apparatus for providing a warning signal to a host system that a circuit card is in the process of being inserted into a card slot of the host system in order to allow the host system to accept the circuit card in an orderly manner that does not adversely affect the host system by protecting the host system from transients that could result from the connection of the circuit card, the circuit card having a connector with a multiplicity of terminals distributed along the connector's width, and arranged in at least one row, for connecting to corresponding terminals of a mating connector in a host system card slot, the circuit card connector having a group of preassigned ground terminals located near both edges of the connector width and a group of preassigned insertion detection terminals located near both edges to be used for card insertion detection, the apparatus comprising:

(a) a card slot connector with connector terminals for mating the card slot connector terminals with a circuit card connector terminals;

(b) detection circuitry connected to the card insertion detection terminals of the card slot connector for generating the warning signal indicating the onset of a circuit card insertion by sensing the grounding of at least one terminal of the card slot connector terminals; and

(c) grounding circuitry that grounds at least one card insertion detection terminal after the circuit card insertion is detected.

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Generate Collection Print

L8: Entry 13 of 13 File: USPT Jun 3, 1997

US-PAT-NO: 5636347
DOCUMENT-IDENTIFIER: US 5636347 A

TITLE: Computer card insertion detection circuit

DATE-ISSUED: June 3, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Muchnick; Michael J.	Fair Oaks	CA		
Verseput; Jerry A.	Folsom	CA		
Ajanovic; Jasmin	Folsom	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 733335 [PALM]
DATE FILED: October 17, 1996

PARENT-CASE:
This is a continuation of application Ser. No. 08/313,454, filed Sep. 24, 1994, now abandoned.

INT-CL: [06] G06 F 13/20

US-CL-ISSUED: 395/283; 395/282
US-CL-CURRENT: 710/302

FIELD-OF-SEARCH: 395/282, 395/283

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4245270	January 1981	Busby	361/58
☐	5210855	May 1993	Bartol	395/500
☐	5268592	December 1993	Bellamy et al.	307/43
☐	5317697	May 1994	Husak et al.	395/500
☐	5410717	April 1995	Floro	395/800

ART-UNIT: 235

PRIMARY-EXAMINER: Ray; Gopal C.

ASSISTANT-EXAMINER: Seto; Jeffrey K.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A personal computer (PC) card insertion method and apparatus uses a subset of connector ground terminals and pins, located at either end of the connector, for detecting the onset of a card insertion. The host PC card slot connector has pull-up resistors for keeping the subset of ground terminals at a high logic level (V.sub.CC). Also, the subset of pins are made longer than the signal pins so that when an insertion of a PC card begins, the grounding of one or more of the subset of pins indicates that a PC card insertion has begun, allowing the host system to take the necessary precautions to ensure an orderly acceptance of the card without any undesirable system affects that might otherwise result. Also, a logic network for using the subset of connector terminals as additional grounding connections is provided upon completion of the insertion.

15 Claims, 11 Drawing figures

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L8: Entry 11 of 13 File: USPT Nov 21, 2000

DOCUMENT-IDENTIFIER: US 6151647 A
TITLE: Versatile interface smart card

Detailed Description Text (10):
The reader 16 has a slot 26 that is appropriately dimensioned to receive the card 18. The bottom of the slot has a switch 28, or other form of sensor, to detect when the card is fully inserted into the slot. The interior surface of the slot has a set of mating contacts (not shown), which engage corresponding contacts 20 on the card when it is fully inserted. When the sensor detects that a card is completely inserted into the slot 26 of the reader, it sends a signal which causes the reader to initiate a power-up procedure, described in detail hereinafter.

Current US Original Classification (1):
710/301

L8: Entry 11 of 13 File: USPT Nov 21, 2000

US-PAT-NO: 6151647
DOCUMENT-IDENTIFIER: US 6151647 A

TITLE: Versatile interface smart card

DATE-ISSUED: November 21, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sarat; Jean-Marc	Belmont	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Gemplus				FR	03

APPL-NO: 09/ 048009 [PALM]
DATE FILED: March 26, 1998

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/103; 710/11, 710/102, 710/104, 710/105
US-CL-CURRENT: 710/301; 710/104, 710/105, 710/11

FIELD-OF-SEARCH: 710/103, 710/102, 710/104, 710/105, 710/129, 710/62, 710/8, 710/11

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5581708	December 1996	Iijima	709/213
☐	5594233	January 1997	Kenneth et al.	235/492
☐	5613159	March 1997	Colnot	710/11
☐	5638530	June 1997	Pawate et al.	711/115
☐	5679945	October 1997	Renner et al.	235/492
☐	5721781	February 1998	Deo et al.	380/25
☐	5832240	November 1998	Larsen et al.	710/105

ART-UNIT: 271

PRIMARY-EXAMINER: Etienne; Ario

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, L.L.P.

ABSTRACT:

A smart card that is compatible with multiple different protocols includes a standard set of contacts that comply with the protocols of a published standard, and another contact not designated by the standard which is used to indicate whether the card is to operate in a non-standard mode. When the card is to operate in the non-standard mode, a simple start-up procedure is employed which does not require strict timing constraints, enabling a less expensive interface device to be used. The interface device can be connected to any bus of a computer which operates in accordance with a desired non-standard protocol. Due to the flexibility and functionality offered by smart cards that have microprocessors incorporated therein, the multi-protocol smart card can be used to drive, or otherwise communicate with, any of a variety of peripheral devices, whether or not a personal computer is present in the system.

31 Claims, 9 Drawing figures

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L8: Entry 6 of 13 File: USPT Jul 20, 2004

DOCUMENT-IDENTIFIER: US 6766469 B2
TITLE: Hot-replace of memory

Current US Cross Reference Classification (1):
710/302

CLAIMS:

16. The method of replacing a memory module in a computer system, as set forth in claim 15, wherein the act of connecting the one or more first insertion removal sense pins causes the assertion of a power signal to a power controller.

32. The method of replacing a memory module in a computer system, as set forth in claim 31, wherein the act of connecting the one or more first insertion removal sense pins causes the assertion of a power signal to a power controller.

49. The method of replacing a memory module in a computer system, as set forth in claim 48, wherein the act of connecting the one or more first insertion removal sense pins causes the assertion of a power signal to a power controller.

60. The method of replacing a memory module in a computer system, as set forth in claim 59, wherein the act of connecting the one or more first insertion removal sense pins causes the assertion of a power signal to a power controller.

L8: Entry 6 of 13 File: USPT Jul 20, 2004

US-PAT-NO: 6766469
DOCUMENT-IDENTIFIER: US 6766469 B2

TITLE: Hot-replace of memory

DATE-ISSUED: July 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Larson; John E.	Houston	TX		
MacLaren; John M.	Cypress	TX		
Johnson; Jerome J.	Spring	TX		
Piccirillo; Gary J.	Cypress	TX		
Lester; Robert A.	Tomball	TX		
Post; Christian H.	Spring	TX		
Galloway; Jeffery	The Woodlands	TX		
Anand; Anisha	Houston	TX		
Lai; Ho M.	Spring	TX		
Rose; Eric	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Development Company, L.P.	Houston	TX			02

APPL-NO: 09/ 769783 [PALM]
DATE FILED: January 25, 2001

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application claims priority to Provisional Application Ser. No. 60/177,952, filed on Jan. 25, 2000.

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/7; 714/5, 711/115, 710/302
US-CL-CURRENT: 714/7; 710/302, 711/115, 714/5

FIELD-OF-SEARCH: 714/7, 714/5, 714/3, 711/115, 439/924.1, 439/924.2, 710/302

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5313626	May 1994	Jones et al.	395/575

☐	5331646	July 1994	Krueger et al.	371/40.1
☐	5367669	November 1994	Holland et al.	395/575
☐	5636347	June 1997	Muchnick et al.	710/302
☐	6098132	August 2000	Olarig et al.	710/103
☐	6223301	April 2001	Santeler et al.	714/6
☐	6549969	April 2003	Hsu et al.	710/304
☐	6651138	November 2003	Lai et al.	711/115
☐	6684292	January 2004	Piccirillo et al.	711/106
☐	6700829	March 2004	Abe et al.	365/226
☐	2004/0030952	February 2004	Piccirillo et al.	714/7

ART-UNIT: 2184

PRIMARY-EXAMINER: Beausoliel; Robert

ASSISTANT-EXAMINER: Duncan; Marc M

ABSTRACT:

A method of replacing a memory module in a computer system. Specifically, a method for replacing a memory module in a segment of a redundant memory system, without powering-down the memory system.

63 Claims, 8 Drawing figures

Previous Doc Next Doc Go to Doc#

US-PAT-NO: 6854070

DOCUMENT-IDENTIFIER: US 6854070 B2

TITLE: Hot-upgrade/hot-add memory

---------- KWIC ----------

Detailed Description Text - DETX (32):

The insertion/removal sensor (IRS) may utilize a pin 118A and a pin 118B to detect when a memory cartridge 25 is being installed or removed. For example, the pin 118A may be made shorter relative to the pin 118B. Additionally, the pin 118B may be made longer than the pins 118C and shorter than the pins 118D and 118E. Thus, during insertion of a memory cartridge 25, the pin 118B will come into contact with a female socket 114B before pins 118A and 118C, but after pins 118D and 118E come into contact with their respective female counterparts. Additionally, during removal of a memory cartridge 25, pin 118B will remain in contact with a female socket 114B longer than pins 118A or 118C. This information may be used by the system 10 to determine when installation or removal of a cartridge 25 has started and when it has been completed. By varying the lengths of the pins 118A-118E, the sequence of signal initialization can be controlled during a hot-plug insertion or removal event.

US006854070B2

(12) **United States Patent**
Johnson et al.

(10) Patent No.: US 6,854,070 B2
(45) Date of Patent: Feb. 8, 2005

(54) **HOT-UPGRADE/HOT-ADD MEMORY**

(75) Inventors: Jerome J. Johnson, Spring, TX (US); John M. MacLaren, Cypress, TX (US); Robert A. Lester, Tomball, TX (US); John E. Larson, Houston, TX (US); Gary J. Piccirillo, Cypress, TX (US); Carlotta H. Post, Spring, TX (US); Jeffery Galloway, The Woodlands, TX (US); Ho M. Lai, Spring, TX (US); Anisha Anand, Houston, TX (US); Eric Rose, Austin, TX (US)

(73) Assignee: Hewlett-Packard Development Company, L.P., Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 596 days.

(21) Appl. No.: 09/769,978

(22) Filed: Jan. 25, 2001

(65) Prior Publication Data

US 2002/0010875 A1 Jan. 24, 2002

Related U.S. Application Data

(60) Provisional application No. 60/177,813, filed on Jan. 25, 2000.

(51) Int. Cl.[7] G06F 11/00

(52) U.S. Cl. 714/5; 714/7; 710/302; 711/115

(58) Field of Search 714/5, 6, 7, 36, 714/42, 54; 711/115; 710/104, 301, 302

(56) References Cited

U.S. PATENT DOCUMENTS

5,313,626	A	5/1994	Jones et al.	395/575
5,331,646	A	7/1994	Krueger et al.	371/40.1
5,357,639	A	10/1994	Nielsen et al.	395/575
5,586,267	A *	1/1996	Lim et al.	713/100
5,491,804	A *	2/1996	Heath et al.	710/7
5,581,712	A *	12/1996	Herman	710/302
5,636,347	A *	6/1997	Machnicki et al.	710/302
5,784,576	A *	7/1998	Guthrie et al.	710/302
6,058,135	A	5/2000	Clardy et al.	710/108
6,223,301	B1	4/2001	Santeler et al.	714/6
6,457,623	B1 *	11/2001	Emerson et al.	710/302
6,604,232	B1 *	8/2003	Bird et al.	716/16

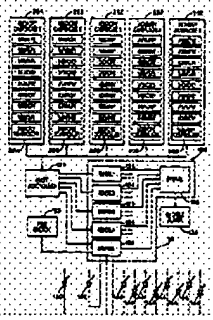
* cited by examiner

Primary Examiner—Dieu-Minh Le

(57) **ABSTRACT**

A method of adding memory capacity to a computer system. The computer system comprises a redundant memory system including a plurality of memory cartridges. By powering-down a memory cartridge, adding an additional memory module to the memory cartridge, and powering-up the memory cartridge for each memory cartridge in the system, the system can transition from a redundant mode of operation to a non-redundant mode of operation for each power-down, thus allowing the computer system to remain functional during the addition of the memory module. Alternatively, memory cartridges with higher memory capacity than those currently present in the computer system can be used to replace existing memory cartridges in the computer system, using the same techniques.

56 Claims, 7 Drawing Sheets



US-PAT-NO: 6766469

DOCUMENT-IDENTIFIER: US 6766469 B2

TITLE: Hot-replace of memory

--------- KWIC ---------

Detailed Description Text - DETX (32):

The insertion/removal sensor (IRS) may utilize a pin 118A and a pin 118B to detect when a memory cartridge 25 is being installed or removed. For example, the pin 118A may be made shorter relative to the pin 118B. Additionally, the pin 118B may be made longer than the pins 118C and shorter than the pins 118D and 118E. Thus, during insertion of a memory cartridge 25, the pin 118B will come into contact with a female socket 114B before pins 118A and 118C, but after pins 118D and 118E come into contact with their respective female counterparts. Additionally, during removal of a memory cartridge 25, pin 118B will remain in contact with a female socket 114B longer than pins 118A or 118C. This information may be used by the system 10 to determine when installation or removal of a cartridge 25 has started and when it has been completed. By varying the lengths of the pins 118A-118E, the sequence of signal initialization can be controlled during a hot-plug insertion or removal event.

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 7 of 7 returned.

1. Document ID: US 6266724 B1

L1: Entry 1 of 7 File: USPT Jul 24, 2001

US-PAT-NO: 6266724
DOCUMENT-IDENTIFIER: US 6266724 B1

TITLE: Removable mother/daughter peripheral card

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

2. Document ID: US 6131134 A

L1: Entry 2 of 7 File: USPT Oct 10, 2000

US-PAT-NO: 6131134
DOCUMENT-IDENTIFIER: US 6131134 A

TITLE: Hot plug-and-play converter of a universal serial bus interface

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

3. Document ID: US 5721669 A

L1: Entry 3 of 7 File: USPT Feb 24, 1998

US-PAT-NO: 5721669
DOCUMENT-IDENTIFIER: US 5721669 A

TITLE: Gear-driven docking apparatus for removable mass-storage drives

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

4. Document ID: US 5717571 A

L1: Entry 4 of 7 File: USPT Feb 10, 1998

US-PAT-NO: 5717571
DOCUMENT-IDENTIFIER: US 5717571 A

TITLE: Mechanism locking removable module into computer

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 5. Document ID: US 5045960 A

L1: Entry 5 of 7 File: USPT Sep 3, 1991

US-PAT-NO: 5045960
DOCUMENT-IDENTIFIER: US 5045960 A

TITLE: Self-aligning guide and track for removable disk drive module

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 5010426 A

L1: Entry 6 of 7 File: USPT Apr 23, 1991

US-PAT-NO: 5010426
DOCUMENT-IDENTIFIER: US 5010426 A

TITLE: Installation mechanism for removable computer drive module

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 4941841 A

L1: Entry 7 of 7 File: USPT Jul 17, 1990

US-PAT-NO: 4941841
DOCUMENT-IDENTIFIER: US 4941841 A

TITLE: Adapter and a removable slide-in cartridge for an information storage system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
4941841.pn. or 5010426.pn. or 5045960.pn. or 5717571.pn. or 5721669.pn. or 6266724.pn. or 6131134.pn.	7

Display Format: TI Change Format

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L6: Entry 1 of 26 File: USPT May 10, 2005

DOCUMENT-IDENTIFIER: US 6892271 B2
TITLE: Memory module resync

Detailed Description Text (30):
In the illustrated embodiment, the memory hot plug interface 110 utilizes various inputs and programmable array logic (PAL) devices 112 to control power to each memory segment 24, illustrated as memory cartridges 25 in FIG. 5. The PAL arrangement 112 receives input from several sources. In the illustrated embodiment, female pins 114A-114E on a cartridge connector 116, which may reside on the memory cartridge 25, are configured to engage male pins 118A-118E on a memory control board 120. Each pin connection provides an electrical path to exchange data and control signals between the memory cartridge 25 and the memory control board 120. For example, an insertion/removal sensor (IRS) and a pre-insertion/removal notification sensor (PIRN) are used to provide inputs to the system.

Detailed Description Text (33):
The insertion/removal sensor (IRS) may utilize a pin 118A and a pin 118B to detect when a memory cartridge 25 is being installed or removed. For example, the pin 118A may be made shorter relative to the pin 118B. Additionally, the pin 118B may be made longer than the pins 118C and shorter than the pins 118D and 118E. Thus, during insertion of a memory cartridge 25, the pin 118B will come into contact with a female socket 114B before pins 118A and 118C, but after pins 118D and 118E come into contact with their respective female counterparts. Additionally, during removal of a memory cartridge 25, pin 118B will remain in contact with a female socket 114B longer than pins 118A or 118C. This information may be used by the system 10 to determine when installation or removal of a cartridge 25 has started and when it has been completed. By varying the lengths of the pins 118A-118E, the sequence of signal initialization can be controlled during a hot-plug insertion or removal event.

Current US Cross Reference Classification (1):
710/302

L6: Entry 3 of 26 File: USPT Feb 8, 2005

DOCUMENT-IDENTIFIER: US 6854070 B2
TITLE: Hot-upgrade/hot-add memory

Detailed Description Text (29):
In the illustrated embodiment, the memory hot plug interface 110 utilizes various inputs and programmable array logic (PAL) devices 112 to control power to each memory segment 24, illustrated as memory cartridges 25 in FIG. 5. The PAL arrangement 112 receives input from several sources. In the illustrated embodiment, female pins 114A-114E on a cartridge connector 116, which may reside on the memory cartridge 25, are configured to engage male pins 118A-118E on a memory control board 120. Each pin connection provides an electrical path to exchange data and control signals between the memory cartridge 25 and the memory control board 120. For example, an insertion/removal sensor (IRS) and a pre-insertion/removal notification sensor (PIRN) are used to provide inputs to the system.

Detailed Description Text (32):
The insertion/removal sensor (IRS) may utilize a pin 118A and a pin 118B to detect when a memory cartridge 25 is being installed or removed. For example, the pin 118A may be made shorter relative to the pin 118B. Additionally, the pin 118B may be made longer than the pins 118C and shorter than the pins 118D and 118E. Thus, during insertion of a memory cartridge 25, the pin 118B will come into contact with a female socket 114B before pins 118A and 118C, but after pins 118D and 118E come into contact with their respective female counterparts. Additionally, during removal of a memory cartridge 25, pin 118B will remain in contact with a female socket 114B longer than pins 118A or 118C. This information may be used by the system 10 to determine when installation or removal of a cartridge 25 has started and when it has been completed. By varying the lengths of the pins 118A-118E, the sequence of signal initialization can be controlled during a hot-plug insertion or removal event.

Current US Cross Reference Classification (1):
710/302

CLAIMS:

27. The method of increasing the memory capacity in a computer system, as set forth in claim 26, wherein the act of connecting the one or more first insertion removal sense pins causes the assertion of a power signal to a power controller.

50. The method of increasing the memory capacity in a computer system, as set forth in claim 49, wherein the act of connecting the one or more first insertion removal sense pins causes the assertion of a power signal to a power controller.

L6: Entry 3 of 26 File: USPT Feb 8, 2005

US-PAT-NO: 6854070
DOCUMENT-IDENTIFIER: US 6854070 B2

TITLE: Hot-upgrade/hot-add memory

DATE-ISSUED: February 8, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Johnson; Jerome J.	Spring	TX		
MacLaren; John M.	Cypress	TX		
Lester; Robert A.	Tomball	TX		
Larson; John E.	Houston	TX		
Piccirillo; Gary J.	Cypress	TX		
Post; Christian H.	Spring	TX		
Galloway; Jeffery	The Woodlands	TX		
Lai; Ho M.	Spring	TX		
Anand; Anisha	Houston	TX		
Rose; Eric	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Development Company, L.P.	Houston	TX			02

APPL-NO: 09/ 769978 [PALM]
DATE FILED: January 25, 2001

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application claims priority to Provisional Application Ser. No. 60/177,812, filed on Jan. 25, 2000. The following commonly owned applications and patents are hereby incorporated by reference for all purposes: U.S. patent application Ser. No. 08/940,419, filed Sep. 30, 1997, entitled "Installation and Removal of Components of a Computer" by Sompong P. Olarig, Kenneth A. Jansen, and Paul A. Sander, issued Aug. 1, 2000, as U.S. Pat. No. 6,098,132; U.S. patent application Ser. No. 08/940,282, filed Sep. 30, 1997, entitled "Fault Tolerant Memory" by Paul A. Santler, Kenneth A. Jansen, and Sompong P. Olarig. U.S. patent application Ser. No. 09/303,369, filed Apr. 30, 1999, entitled "Replacement, Upgrade and/or Additional of Hot-Pluggable Components in a Computer System" by Theodore F. Emerson, Vincent Nguyen, Peter Michels, and Steve Clohset; and U.S. patent application Ser. No. 09/769,956, filed Jan. 25, 2001, entitled "Memory Sub-System Error Cleansing" by William J. Walker, and John M. MacLaren; U.S. patent application Ser. No 09/769,716, filed Jan. 25, 2001, entitled "Hot Replace Power Control Sequence Logic" by John M. MacLaren, Jerome J. Johnson, Robert A. Lester, Gary J. Piccirillo, John E. Larson, and Christian H. Post; U.S. patent application Ser. No. 09/769,783, filed Jan. 25, 2001, entitled "Hot-Replace of Memory" by John E. Larson, John M. MacLaren, Jerome J. Johnson, Gary J. Piccirillo, Robert A. Lester, Christian H. Post, Jefferey Galloway, Anisha Anand, Ho M. Lai, and Eric Rose; U.S. patent application Ser. No. 09/769,978, filed Jan. 25, 2001, entitled "Hot-Upgrade/Hot-Add Memory" by Jerome J. Johnson, John M. MacLaren, Robert A. Lester, John E. Larson, Gary J. Piccirillo, Christian H. Post, Jeffery Galloway, Ho M. Lai, Anisha Anand, and Eric Rose; U.S. patent application Ser. No. 09/769,957, filed Jan. 25, 2001, entitled "Raid Memory" by John M. MacLaren, Paul Santeler, Kenneth A. Jansen, Sompong P. Olarig, Robert A.

Lester, Patrick L. Ferguson, John E. Larson, Jerome J. Johnson, and Gary J. Piccirillo; U.S. patent application Ser. No. 09/769,833, filed Jan. 25, 2001, entitled "Technique for Identifying Multiple Circuit Components" by John M. MacLaren and John E. Larson; U.S. patent application Ser. No. 09/769,958, filed Jan. 25, 2001, entitled "Memory Data Verify Operation" by Robert A. Lester, John M. MacLaren, Patrick L. Ferguson, and John E. Larson; U.S. patent application Ser. No. 09/769,959, filed Jan. 25, 2001, entitled "Real-Time Hardware Memory Scrubbing" by John E. Larson, John M. MacLaren, Robert A. Lester, Gary Piccirillo, Jerome J. Johnson, and Patrick L. Ferguson; U.S. patent application Ser. No. 09/770,101, filed Jan. 25, 2001, entitled "Hot-Plug Memory Cartridge Power Control Logic" by Ho M. Lai and John M. MacLaren; U.S. patent application Ser. No. 09/770,100, filed Jan. 25, 2001, entitled "Removable Memory Cartridge System for Use With a Server or Other Processor-Based Device" by Brett D. Roscoe, George D. Megason, and Christian H. Post.

INT-CL: [07] G06F01100

US-CL-ISSUED: 714/5; 714/7, 710/302, 711/115
US-CL-CURRENT: 714/5; 710/302, 711/115, 714/7

FIELD-OF-SEARCH: 714/5, 714/6, 714/7, 714/36, 714/42, 714/54, 711/115, 710/104, 710/301, 710/302

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5313626	May 1994	Jones et al.	395/575
☐	5331646	July 1994	Krueger et al.	371/40.1
☐	5367669	November 1994	Holland et al.	395/575
☐	5386567	January 1995	Lien et al.	713/100
☐	5491804	February 1996	Heath et al.	710/7
☐	5581712	December 1996	Herrman	710/302
☐	5636347	June 1997	Muchnick et al.	710/302
☐	5784576	July 1998	Guthrie et al.	710/302
☐	6098132	August 2000	Olarig et al.	710/103
☐	6223301	April 2001	Santeler et al.	714/6
☐	6487623	November 2002	Emerson et al.	710/302
☐	6604152	August 2003	Bard et al.	710/16

ART-UNIT: 2114

PRIMARY-EXAMINER: Le; Dieu-Minh

ABSTRACT:

A method of adding memory capacity to a computer system. The computer system comprises a redundant memory system including a plurality of memory cartridges. By powering-down a memory cartridge, adding an additional memory module to the memory cartridge, and powering-up the memory cartridge for each memory cartridge in the system, the system can transition from a

redundant mode of operation to a non-redundant mode of operation for each power-down, thus allowing the computer system to remain functional during the addition of the memory module. Alternatively, memory cartridges with higher memory capacity than those currently present in the computer system can be used to replace existing memory cartridges in the computer system, using the same techniques.

56 Claims, 8 Drawing figures

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L6: Entry 17 of 26 File: USPT Mar 6, 2001

DOCUMENT-IDENTIFIER: US 6199128 B1
TITLE: Smart card system for use with peripheral devices

Detailed Description Text (10):
The reader 16 has a slot 26 that is appropriately dimensioned to receive the card 18. The bottom of the slot has a switch 28, or other form of sensor, to detect when the card is fully inserted into the slot. The interior surface of the slot has a set of mating contacts (not shown), which engage corresponding contacts 20 on the card when it is fully inserted. When the sensor detects that a card is completely inserted into the slot 26 of the reader, it sends a signal which causes the reader to initiate a power-up procedure, described in detail hereinafter.

Current US Original Classification (1):
710/301

L6: Entry 17 of 26 File: USPT Mar 6, 2001

US-PAT-NO: 6199128
DOCUMENT-IDENTIFIER: US 6199128 B1

TITLE: Smart card system for use with peripheral devices

DATE-ISSUED: March 6, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sarat; Jean-Marc	Belmont	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Gemplus, S.C.A.				FR	03

APPL-NO: 09/ 048010 [PALM]
DATE FILED: March 26, 1998

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/102; 710/129, 710/2, 710/72
US-CL-CURRENT: 710/301; 710/2, 710/72

FIELD-OF-SEARCH: 235/25, 235/380-386, 235/492, 380/25, 380/23, 710/1-14, 710/36-51, 710/72-74, 710/100-106, 710/126-131

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4985920	January 1991	Seki	380/23
☐	5093862	March 1992	Scwartz	380/25
☐	5434395	July 1995	Storck et al.	235/380
☐	5521362	May 1996	Powers	235/380
☐	5721781	February 1998	Deo et al.	380/25
☐	5729004	March 1998	Kim et al.	235/492
☐	5834756	November 1998	Gutman et al.	235/493
☐	5841868	November 1998	Helbig, Sr.	380/25
☐	5852290	December 1998	Chaney	235/492
☐	6012634	January 2000	Brogan et al.	235/380

ART-UNIT: 272

PRIMARY-EXAMINER: Shin; Christopher B.

ATTY-AGENT-FIRM: Burns, Doane, Swecker & Mathis, L.L.P.

ABSTRACT:

A smart card that is compatible with multiple different protocols includes a standard set of contacts that comply with the protocols of a published standard, and another contact not designated by the standard which is used to indicate whether the card is to operate in a non-standard mode. When the card is to operate in the non-standard mode, a simple start-up procedure is employed which does not require strict timing constraints, enabling a less expensive interface device to be used. The interface device can be connected to any bus of a computer which operates in accordance with a desired non-standard protocol. Due to the flexibility and functionality offered by smart cards that have microprocessors incorporated therein, the multi-protocol smart card can be used to drive, or otherwise communicate with, any of a variety of peripheral devices, whether or not a personal computer is present in the system.

24 Claims, 9 Drawing figures

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L1: Entry 5 of 5 File: USPT Aug 27, 2002

DOCUMENT-IDENTIFIER: US 6442734 B1

** See image for Certificate of Correction **

TITLE: Method and apparatus for detecting the type of interface to which a peripheral device is connected

Detailed Description Text (26):

Switch controller 146 then turns on switch 150 to enable pull-up resistor 154. It should be noted that the particular pull-up resistor enabled at this point is that pull-up resistor which is connected to the PS2 data conductor and the USB D+ conductor for a high-speed USB device, or the PS2 data conductor and the USB D- conductor for a low-speed USB device. The flow diagram illustrated in FIG. 4 illustrates operation of the PS2/high-speed USB peripheral device.

Detailed Description Text (36):

Microcontroller 202 also includes USB differential data outputs D+ and D- provided on pins 226 and 228. The D+ and D- pins 226 and 228 are coupled to conductors which represent USB D+ and USB D- signals for a high-speed USB device, and PS2 data and PS2 clock signals, respectively, for a PS2 device.

Detailed Description Text (48):

As with FIG. 4, the signals mentioned in FIG. 6 can be combined differently such that either the PS2 data or PS2 clock signals can be associated with either the USB D+ or USB D- signals. This type of system is contemplated to be within one illustrative embodiment of the present invention.

Generate Collection Print

L1: Entry 5 of 5 File: USPT Aug 27, 2002

US-PAT-NO: 6442734
DOCUMENT-IDENTIFIER: US 6442734 B1
** See image for Certificate of Correction **

TITLE: Method and apparatus for detecting the type of interface to which a peripheral device is connected

DATE-ISSUED: August 27, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hanson; Mark T.	Lynnwood	WA		
Sherman; Nathan C.	Redmond	WA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Microsoft Corporation	Redmond	WA			02

APPL-NO: 09/ 410413 [PALM]
DATE FILED: October 1, 1999

PARENT-CASE:
REFERENCE TO CO-PENDING APPLICATION This is a continuation-in-part of the application Ser. No. 09/112,171, filed Jul. 8, 1998 entitled "METHOD AND APPARATUS FOR DETECTING THE TYPE OF INTERFACE TO WHICH A PERIPHERAL DEVICE IS CONNECTED" and assigned the same assignee as the present invention.

INT-CL: [07] G06 F 17/50

US-CL-ISSUED: 716/4
US-CL-CURRENT: 716/4

FIELD-OF-SEARCH: 710/129, 710/100, 710/15, 710/63, 710/62, 710/110, 710/8, 326/30, 360/69, 708/854, 713/400, 716/1, 716/4, 716/5, 716/6, 716/12

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4500933	February 1985	Chan	360/69
☐	4785469	November 1988	Joshi et al.	375/110
☐	5043938	August 1991	Ebersole	364/900
☐	5473264	December 1995	Mader et al.	326/30

☐	5481696	January 1996	Lomp et al.	395/500
☐	5548782	August 1996	Michael et al.	395/835
☐	5577213	November 1996	Avery et al.	395/280
☐	5612634	March 1997	MacKenna	326/62
☐	5644790	July 1997	Li et al.	395/883
☐	5754890	May 1998	Holmdahl et al.	
☐	5793999	August 1998	Mori	395/309
☐	5828905	October 1998	Rao	395/883
☐	5832244	November 1998	Jolley et al.	395/309
☐	5857112	January 1999	Hashemi et al.	395/828
☐	5928347	July 1999	Jones	710/129
☐	5935224	August 1999	Svancarek et al.	710/63
☐	6006295	December 1999	Jones et al.	710/62

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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 860 781	February 1998	EP	
WO 97/31386	August 1997	WO	
WO 97/17214	April 1999	WO	

OTHER PUBLICATIONS

Universal Serial Bus Specification, Rev 1.1, Section 7.1.5: Device speed identification, pp. 113 and 114, Sep. 23, 1998.

ART-UNIT: 2825

PRIMARY-EXAMINER: Smith; Matthew

ASSISTANT-EXAMINER: Do; Thuan

ATTY-AGENT-FIRM: Kelly; Joseph R. Westman, Champlin & Kelly, P.A.

ABSTRACT:

A peripheral device is connectable to a computer having one of a first interface and a second interface. The first interface communicates with the peripheral device over a differential data connection having a first data conductor and a second data conductor. The second interface communicates with the peripheral device over a clock conductor and a single ended data connection which includes a data conductor. The peripheral device has first and second communication conductors configured for connection to the first and second data conductors in the differential data connection when the computer includes the first interface and is configured for connection to the first data conductor in the single ended data connection and the clock conductor when the computer is provided with the second interface. The peripheral device includes an interface detection component coupled to the first and second communication conductors and configured to detect which of the first and second interfaces the peripheral device is connected to. The peripheral device also includes a controller component configured to communicate between the peripheral device according to a protocol corresponding to the detected interface.

51 Claims, 9 Drawing figures